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Inventor: Valerie L. Lines

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DYNAMIC MEMORY WORD LINE DRIVER SCHEME

RELATED APPLICATIONS

This application is a Continuation of Application No. 10/463,194, filed on June 17, 2003, which is a Continuation of Application No. 09/919,752, filed on July 31, 2001, now U.S. Patent No. 6,603,703, which issued on August 5, 2003, which is a Continuation of Application No. 09/548,879, filed on April 13, 2000, now U.S. Patent No. 6,278,640, which issued on August 21, 2001, which is a Continuation of Application No. 09/123,112, filed on July 27, 1998, now U.S. Patent No. 6,061,277, which issued on May 9, 2000, which is a Continuation of Application No. 08/705,534, filed on August 29, 1996, now abandoned, which is a Continuation of Application No. 08/611,558, filed on March 6, 1996, now U.S. Patent No. 5,751,643, which issued on May 12, 1998, which is a Continuation-in-Part of Application No. 08/515,904, filed on August 16, 1995, now U.S. Patent No. 5,822,253, which issued on October 13, 1998, which is a Continuation of Application No. 08/205,776, filed on March 3, 1994, now abandoned, which is a File Wrapper Continuation of Application No. 08/031,898, filed on March 16, 1993, now abandoned, which is a Continuation of Application No. 07/680,746, filed on April 5, 1991, now U.S. Patent No. 5,214,602, which issued on May 25, 1993, which relates to Japanese Application No. 9107165, filed on April 5, 1991 and United Kingdom Application No. 9007790.0, filed on April 6, 1990. The entire teachings of the above applications are incorporated herein by reference.

FIELD OF THE INVENTION:

This invention relates to CMOS dynamic random access memories (DRAMs), and particularly to word line drivers.

BACKGROUND TO THE INVENTION:

Dynamic random access memories are generally formed of a matrix of bit lines and word lines with memory cells located adjacent the intersections of the bit lines and word lines. The memory cells are enabled to provide their stored bits to the bit lines or to permit a write operation by signals carried on the word lines.

Each memory cell is typically formed of a bit storage capacitor connected to a reference voltage and through the source-drain circuit of an "access" field effect transistor to an associated bit line. The gate of the field effect transistor is connected to the word line. A logic signal carried by the word line enables the transistor, thus allowing charge to flow through the source-drain circuit of the transistor to the capacitor, or allowing charge stored on the capacitor to pass through the source-drain circuit of the access transistor to the bit line.

In order for the logic level V_{dd} potential from the bit line to be stored on the capacitor, the word line must be driven to a voltage above $V_{dd}+V_{tn}$, where V_{tn} is the threshold voltage of the access transistor including the effects of back bias.

During the early days of DRAM design, NMOS type FETs, that is, N-channel devices were used exclusively. In order to pass a $V_{dd} + V_{tn}$ level signal to the selected word line, the gate of the pass transistor had to be driven to at least $V_{dd}+2V_{tn}$. Furthermore, to allow sufficient drive to achieve a voltage greater than $V_{dd}+V_{tn}$ on the word line within a

reasonable length of time in order to facilitate a relatively fast memory, the gate of the pass transistor is driven to a significantly higher voltage. In such devices, the word line driving signal utilized capacitors in a well-known double-boot strap circuit.

In the above circuit, the boot strapping voltage circuit is designed to exceed the voltage $V_{dd}+2V_{tn}$, in order to ensure that temperature, power supply, and process variations would never allow the pass transistor driving voltage to fall below $V_{dd}+2V_{tn}$.

However, it has been found that in small geometry VLSI memories, the high voltages provided by the boot-strap circuits can exceed the tolerable voltages in the memory, thus adversely affecting reliability.

SUMMARY OF THE INVENTION:

The present invention is a circuit which accurately controls the word line (pass transistor gate) driving voltage to a voltage which is both controlled and is not significantly greater than is needed to drive the word line. The elements of the present invention eliminate the need for a double-boot-strapping circuit, and ensure that no voltages exceed that necessary to fully turn on a memory cell access transistor. Accordingly, voltages in excess of that which would reduce reliability are avoided, and accurate driving voltages are obtained.

According to an embodiment of the invention a dynamic random access memory (DRAM) is comprised of word lines, memory cells having enable inputs connected to the word lines, apparatus for receiving word line selecting signals at first logic levels V_{ss} and V_{dd}, and for providing a select signal at levels V_{ss} and V_{dd}, a high voltage supply source V_{pp} which is higher in voltage than V_{dd}, a circuit for

translating the select signals at levels V_{ss} and V_{dd} to levels V_{ss} and V_{pp} and for applying it directly to the word lines for application to the enable inputs whereby an above V_{dd} voltage level word line is achieved without the use of double boot-strap circuits.

According to another embodiment, a dynamic random access memory (DRAM) is comprised of bit lines and word lines, memory cells connected to the bit lines and word lines, each memory cell being comprised of an access field effect transistor (FET) having its source-drain circuit connected between a bit line and a bit charge storage capacitor, the access field effect transistor having a gate connected to a corresponding word line; a high supply voltage source V_{pp}; a circuit for selecting the word line and a circuit having an input driven by the selecting apparatus for applying the V_{pp} supply voltage to the word line.

BRIEF INTRODUCTION TO THE DRAWINGS:

A better understanding of the invention will be obtained by reference to the detailed description below, in conjunction with the following drawings, in which:

Figure 1 is a schematic diagram of the invention.

DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION:

Turning now to Figure 1, a CMOS DRAM is comprised of word lines, represented by word line 1 and bit lines, represented by bit lines 2A, 2B, etc. Access transistors 3A, 3B have their gates connected to the word line; their sources are connected to bit charge storing capacitors 4A, 4B, etc. which are also connected to ground. The drains of access transistors 3A, 3B, etc. are connected to the bit lines 2A, 2B, etc.

With the application of a logic signal of $V_{dd}+V_{tn}$ to the gate of transistor 3A, 3B, etc., V_{dd} level on the bit line 2A, 2B, etc. is fully transferred to the associated capacitor 4A, 4B, etc. during the writing cycle. In the prior art it was necessary to apply a voltage greater than $V_{dd}+2V_{tn}$ to the gate of an N-channel pass transistor in order to ensure that a voltage in excess of $V_{dd}+V_{tn}$ would be available at the gates of transistors 3A, 3B, etc.

The combination of a bit storing charge capacitor, e.g. 4A, with an associated access transistor, e.g. 3A, forms a memory cell in prior art DRAMs.

The word line is selected by means of addresses A_{ij} applied to the inputs of a NAND gate 5. In the prior art a double boot-strap circuit was connected between the output of NAND gate 5 and the word line.

In accordance with the present invention a voltage V_{pp} which is higher than the logic level $V_{dd}+V_{tn}$ is utilized. A level shifter 6 is formed of a pair of cross coupled P-channel transistors 7A and 7B. The sources of transistors 7A and 7B are connected to the voltage source V_{pp}. The level shifter defines a first and a second control node, respectively 8A and 8B.

The output of NAND gate 5 is connected through an inverter 9 to the gate of an N-channel FET 10. FET 10 has its source connected to ground and its drain connected to control node 8A.

The output of NAND gate 5 is connected to the gate of an N-channel FET 11, which has its source connected to ground and its drain connected to control node 8B. A third N-channel FET 12 has its source connected to ground, its drain connected to the drain of transistor 11, and its gate to control node 8A.

Control node 8A (or a buffered version of control node 8A) is applied to the gate of pass transistor 14A and pull down transistor 13A. The source of pass transistor 14A is connected to V_{pp} or to a secondary decoder output which provides a V_{ss} or V_{pp} level output; its drain to word line 1. The source of pull down transistor 13A is connected to ground; the drain is connected to word line 1.

In operation, assume that the word line 1 has not been selected. At least one address input of NAND gate 5 is low, causing the output of NAND gate 5 to be high, and the output of inverter 9 to be low. Transistor 11 is enabled, pulling node 8B to ground. Transistor 10 is disabled, allowing transistor 7A to charge node 8A to V_{pp}. Transistor 12 is thus enabled ensuring that node 8A is pulled high. The V_{pp} level node 8A disables the pass device 14A and enables pull down transistor 13A so that word line 1 is held at ground. Thus transistors 3A and 3B are not enabled and are not conducting. The charge stored on capacitors 4A and 4B are thus maintained, and are not read to the bit lines.

Assume now that word line 1 is selected. Logic high level address signals at the voltage level V_{dd} are applied to the inputs of NAND gate 5. The output of the NAND gate thus goes to low level. The output of inverter 9 changes to high level, transistor 10 is enabled, and pulls node 8A toward ground. This causes transistor 7B to be enabled, and pull node 8B toward V_{pp}. This causes transistor 7A to be disabled so that node 8A is pulled to ground, disabling transistor 12 and allowing transistor 7B to charge node 8B to V_{pp}. The ground level voltage on node 8A disables pull down transistor 13A, and enables the pass transistor 14A so that the word line 1 is driven to a V_{pp} level. The voltage on the word line is thus controlled, and depending on whether the

word line is selected or not, it switches between ground and V_{pp}. With the voltage V_{pp} being controlled to $V_{dd}+V_{tn}$, the voltage at the gates of the cell access transistors 3A and 3B is certain to be $V_{dd}+V_{tn}$. However the voltage V_{pp} is selected to be less than a voltage that would be in excess of that which would deteriorate reliability of the DRAM.

A person understanding this invention may now conceive of alternative structures and embodiments or variations of the above. All of those which fall within the scope of the claims appended hereto are considered to be part of the present invention.